Remarks:

      Claims 43-45 and 47 are pending in the current application and are rejected under 35 U.S.C. §102(e). Claims 43 and 47 are amended. New claims 49-51 have been added. No new matter has been added. Support for the amendments and new claims is found within the claims, the specification and the drawings. It is submitted that the application, as amended, is in condition for allowance. Reconsideration and continued examination are respectfully requested.

§112 Rejection(s):

      Claim 43 is rejected under 35 U.S.C. §112, second paragraph, for lack of antecedent basis. Applicant has amended Claim 43 to recite sufficient antecedent basis for "lines," per Examiner's observation.

§102(e) Rejection(s):

      The Examiner has rejected Claims 43-45 and 47 as being anticipated by US Patent No. 6,342,823 (Dansky et al.) under 35 U.S.C. § 102(e). Applicant respectfully submits that the instant application (Alon) and Dansky are commonly owned and subject to an obligation of assignment to the same person at the time the present invention was made. M.P.E.P. § 715.01(b) provides, in relevant part, "where a rejection is applied … under 35 U.S.C. 102(e)/ 103 using the reference, a showing that the invention was commonly owned, or subject to an obligation of assignment to the same person, at the time the later invention was made would preclude such a rejection or be sufficient to overcome such a rejection. See MPEP § 706.02(l) and § 706.02(l)(1). Accordingly, it is respectfully requested that the rejection of Claims 43-45 and 47 under 35 U.S.C. § 102(e) be withdrawn.

      Further, it is respectfully noted that anticipation of a claim under 35 U.S.C. §102 (a), (b) and (e) requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," that "[t]he identical invention must be shown in as complete detail as is contained in the … claim" and "[t]he elements must be arranged as required by the claim." M.P.E.P. §2131.

      Claim 43, as amended, recites an integrated circuit design library for providing design elements for analog and mixed signal circuits, the library comprising: a set of selectable transmission line topologies selectable as design elements for critical interconnect lines of an integrated circuit being designed, wherein the integrated circuit may be modeled using said critical interconnect lines before the

physical layout of the integrated circuit is determined, said critical interconnect lines defined by a set of geometry parameters and capable of carrying analog and mixed signals, which topologies comprise return paths therein; and a set of parameterized, equivalent RLC ladder networks, one per topology. Claims 50 and 51 recite a method and a computer program product, respectively, for modeling a transmission line topology selectable as a design element for a critical interconnect line of an integrated circuit being designed, and substantially incorporate the elements of Claim 43.

Dansky discloses a method and system for reducing computation complexity and improving accuracy of delay and crosstalk calculation in transmission lines with frequency-dependent losses (Abstract). Particularly, Dansky discloses an analysis tool based on restricted coupled-line technologies, RLC matrix conversion, and prestored synthesized circuits.

Dansky fails to disclose selectable transmission line topologies selectable as design elements for critical interconnect lines of an integrated circuit being designed, wherein the integrated circuit may be modeled using said critical interconnect lines before the physical layout of the integrated circuit is determined. Rather, Dansky discloses extracting critical interconnects using post-routing analysis (i.e., after the physical design stage, where the on-chip physical layout of components are defined), which involves two-dimensional or some limited three-dimensional extraction and additional simulations with subsequent rerouting or circuit design changes (col. 1 lines 46-50; col. 5 lines 18-51).

According to Dansky, a wiring layout is obtained and critical nets, such as macro-to-macro connections, data buses between central-processor-unit (CPU) to cache memory, long control lines, clock lines, are identified (col. 5 lines 21-24). Simulation is performed using synthesized circuits and device information, and if there is an issue (i.e., noise) with a net (i.e., interconnect circuit), the net is flagged (i.e., identified as critical) (col. 5 lines 39-53). Rerouting, buffer circuits, or other design changes to the current layout are made and the entire analysis is then repeated (col. 5 lines 53-59). Thus, Dansky discloses determining critical interconnect lines through *post-layout* element extraction and circuit simulation.

In contrast, Alon is directed to designing the critical interconnect lines from the initial design stages by providing a set of selectable transmission line topologies selectable as design elements, rather than extracting the critical interconnect lines in post layout design stages (see Alon paragraph [0030]). Critical interconnect lines are identified, modeled as transmission lines and incorporated in a netlist from

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the early stages of the design flow (i.e., schematic design stage), as opposed to the post layout design stages, as suggested by Examiner.

Applicant respectfully submits that Dansky, in fact, teaches away from selectable transmission line topologies selectable as design elements for critical interconnect lines of an integrated circuit being designed wherein the integrated circuit may be modeled using said critical interconnect lines before the physical layout of the integrated circuit is determined. Generally, "a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *In re Gurley, supra. see,* also, *In re Caldwell,* 319 F.2d 254, 2656, 138 USPQ 243, 245 (CCPA 1963) (reference teaches away if it leaves the impression that the product would not have the property sought by the applicant).

Dansky suggests determining critical interconnect lines in a post-layout stage, after complex extractions from the physical design stage and running a circuit simulation, and then redesigning a chip layout accordingly. Dansky thus teaches away from the method and library recited in the pending claims where critical interconnect lines are selected and identified and incorporated into the schematic design stage, without having to determine the actual on-chip physical layout of components or performing complex circuit simulations.

Claim 49 recites the library of Claim 43, wherein the RLC ladder networks are constructed by using the set of geometry parameters and a reduced RLC network for the selected topology, such that the equivalent RLC networks may be used by a circuit-level simulator to model said critical interconnect lines, wherein actual RLC values for said reduced RLC network are calculated by using calculated low frequency RLC values and calculated high frequency RLC values, such that said reduced RLC network correctly describes the transmission line topology behavior across a frequency range of interest, wherein the low frequency RLC values are calculated per unit length using a model complying with electrostatic and magnetostatic principles for a geometry parameter range and the high frequency RLC values are calculated per unit length using a quasi-TEM approximation from the capacitance data to calculate a high frequency limit transverse electromagnetic inductance matrix. Claims 50 and 51 substantially incorporate the elements of Claim 49.

Regarding Claims 49-51, Dansky fails to disclose calculating low frequency RLC values per unit length, wherein the low frequency values are calculated using a model complying with electrostatic and magnetostatic principles for a geometry parameter range as claimed. Dansky instead discloses

designating values for circuit elements at low frequency (i.e., zero frequency or DC), namely R_{dC1} and R_{dC2} (col. 3 lines 62-63; col. 4 lines 2-3). Dansky also fails to disclose calculating high frequency RLC values per unit length, wherein a high frequency limit transverse electromagnetic inductance matrix may be calculated from the capacitance using a quasi-TEM approximation, as claimed. Dansky in contrast discloses using a circuit *only* based on the R_{dC} and the high frequency inductance values (col. 5, lines 13-14, emphasis added). The high frequency inductance is *only* calculated at an infinite frequency (col. 4 line 54, emphasis added). Thus, Dansky does not disclose calculating high frequency RLC values using a quasi-TEM approximation as claimed. Further, the claims allow calculations at a low frequency and a high frequency limit, and do not require calculations only at DC or an infinite frequency as disclosed in Dansky.

Additionally, Dansky fails to disclose calculating actual RLC values for a reduced RLC network by using the calculated low frequency RLC values and the calculated high frequency RLC values, wherein the reduced RLC network correctly describes the transmission line topology behavior across a frequency range of interest as recited in the pending claims. Rather, Dansky discloses fitting R and L values using a set of constants obtained from 3D Matrix Extraction based on the R_{dc} and the high frequency (infinite) inductance values (col. 5 lines 8-18).

Dansky also fails to disclose the claimed process for constructing an equivalent RLC network for said transmission line topology using the set of geometry parameters and the reduced RLC network, such that the equivalent RLC network may be used by a circuit-level simulator to model said critical interconnect lines. Rather, Dansky discloses creating a table of RLC values representing presynthesized circuits (i.e., topologies), where R and L's are *precalculated* for a large number of line dimensions and stored in a table (col. 4 lines 55-57, col. 5 lines 13-17, emphasis added). For each circuit configuration (topology), scaling factors are used for conversion from 2D to 3D values (col. 4 lines 49-51). These factors are the *same for each circuit regardless* of line widths, separations, or distance to GND and Vdd buses (col. 4 lines 51-53, emphasis added). Dansky essentially ignores the geometry parameters, and in fact, teaches away from the claimed method where the geometry parameters for each identified critical interconnect line are used to construct the equivalent RLC network, for the purpose of a much more accurate RLC representation.

For the above reasons, Dansky fails to disclose each and every element as set forth in Claim 43, as amended, in as complete detail as is contained in the claim or as required by the claim. Accordingly, it is respectfully requested that the rejection of Claim 43 under 35 U.S.C. § 102 be withdrawn.

Conclusion:

For the above reasons, the invention as recited in the amended Claim 43 is distinguishable over the reference cited by the Examiner. Therefore, Claim 43 should be in condition for allowance. Claims 44-45, 47 and 49 are dependent on Claim 43 and should also be in condition for allowance by the virtue of their dependence on an allowable base claim. New Claims 50 and 51 substantially incorporate the elements of Claim 43 and therefore should also be in condition for allowance.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein; and no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have expressly argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California, telephone number (310) 789-2100 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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